



6549235

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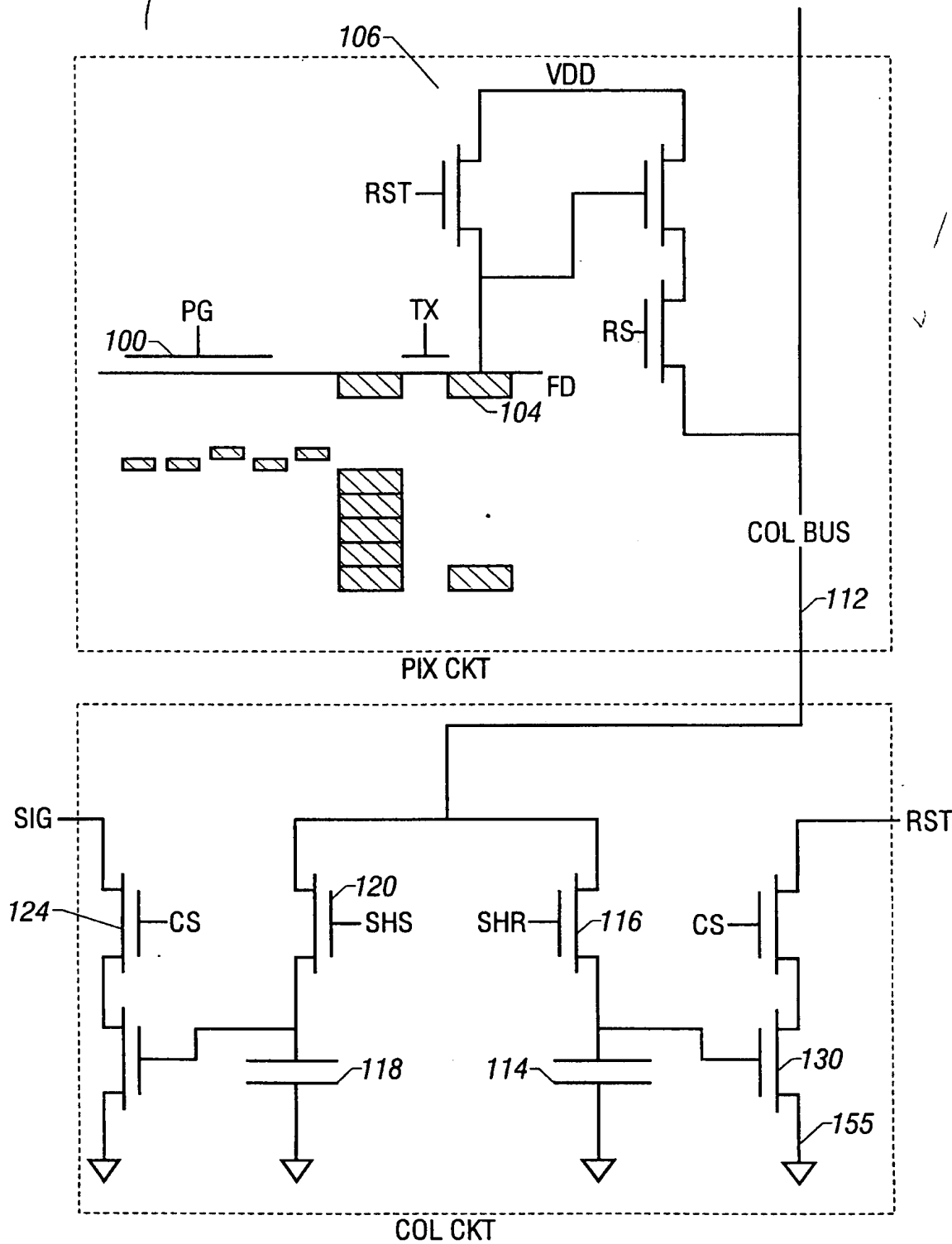


FIG. 1

09.02



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Applicant(s): Eric R. Fossum, et al.

SINGLE SUBSTRATE CAMERA DEVICE WITH CMOS IMAGE  
SENSOR (AS AMENDED)

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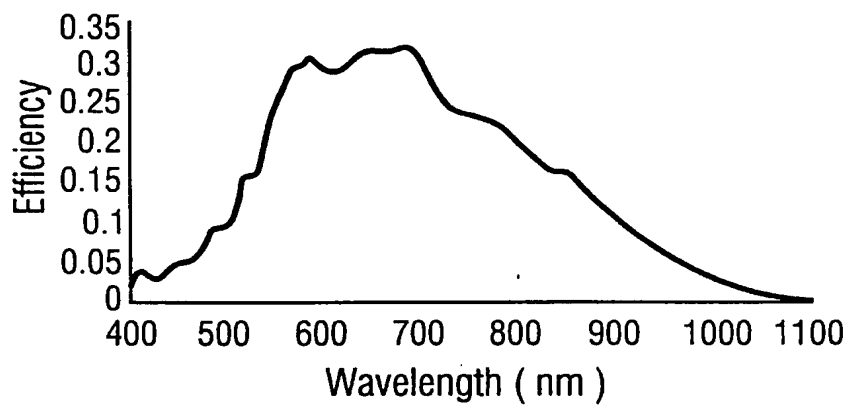
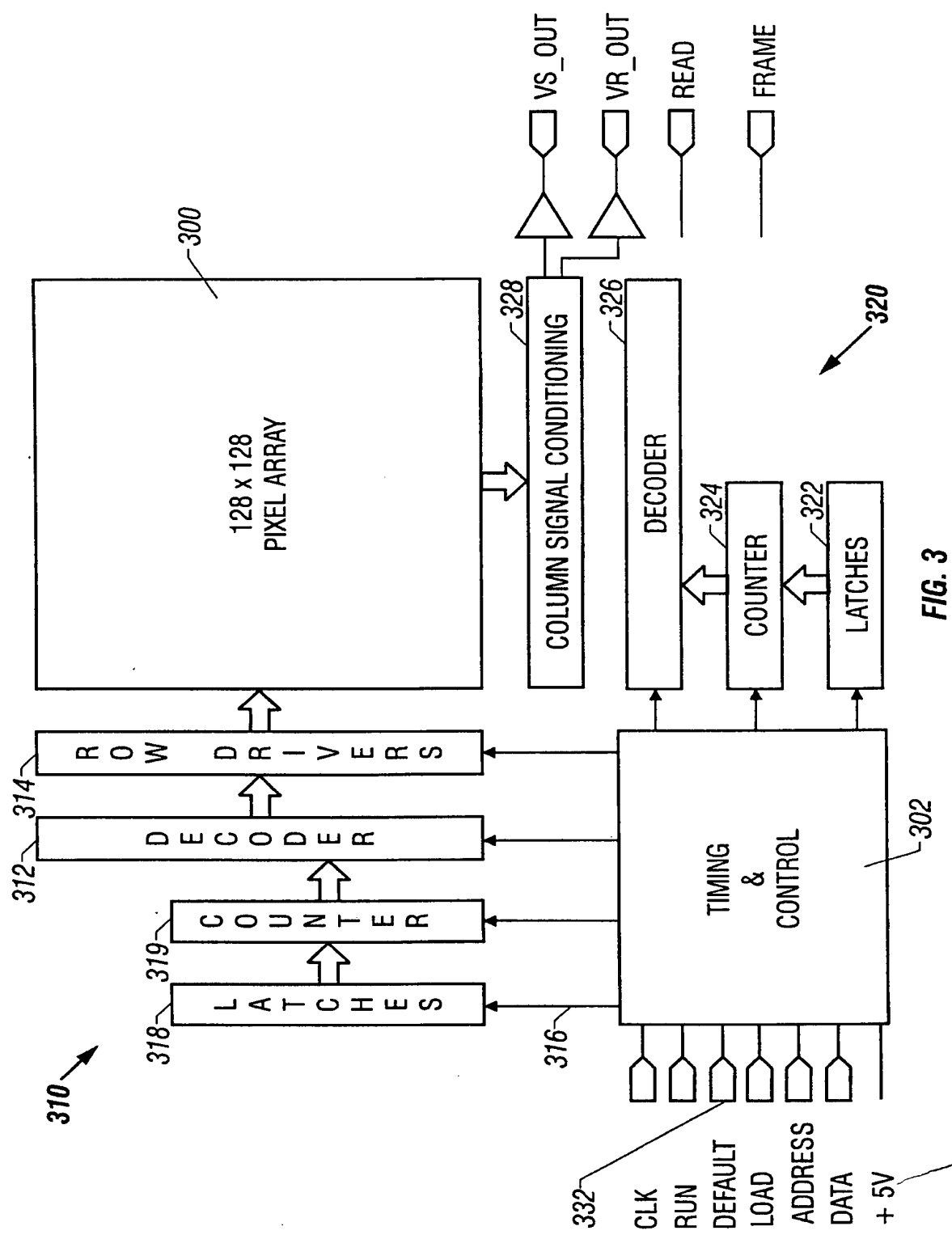


FIG. 2

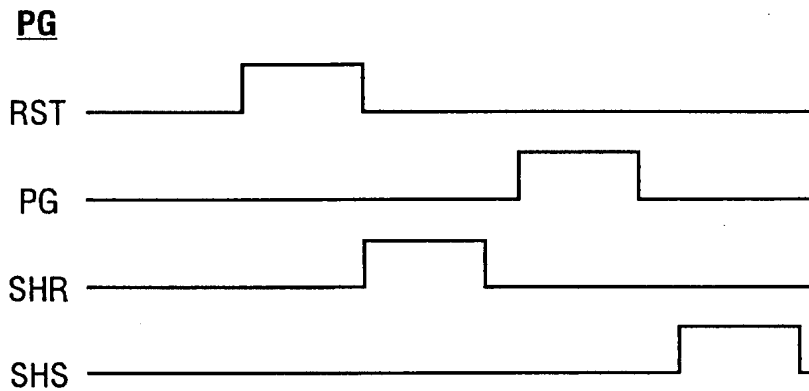


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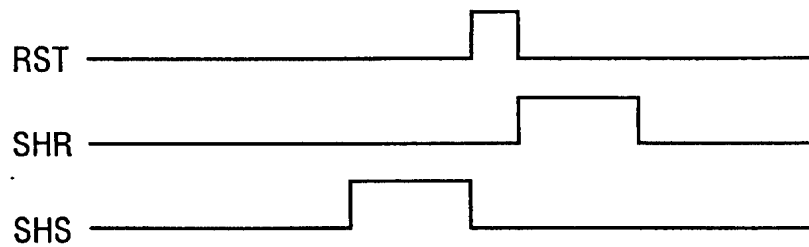




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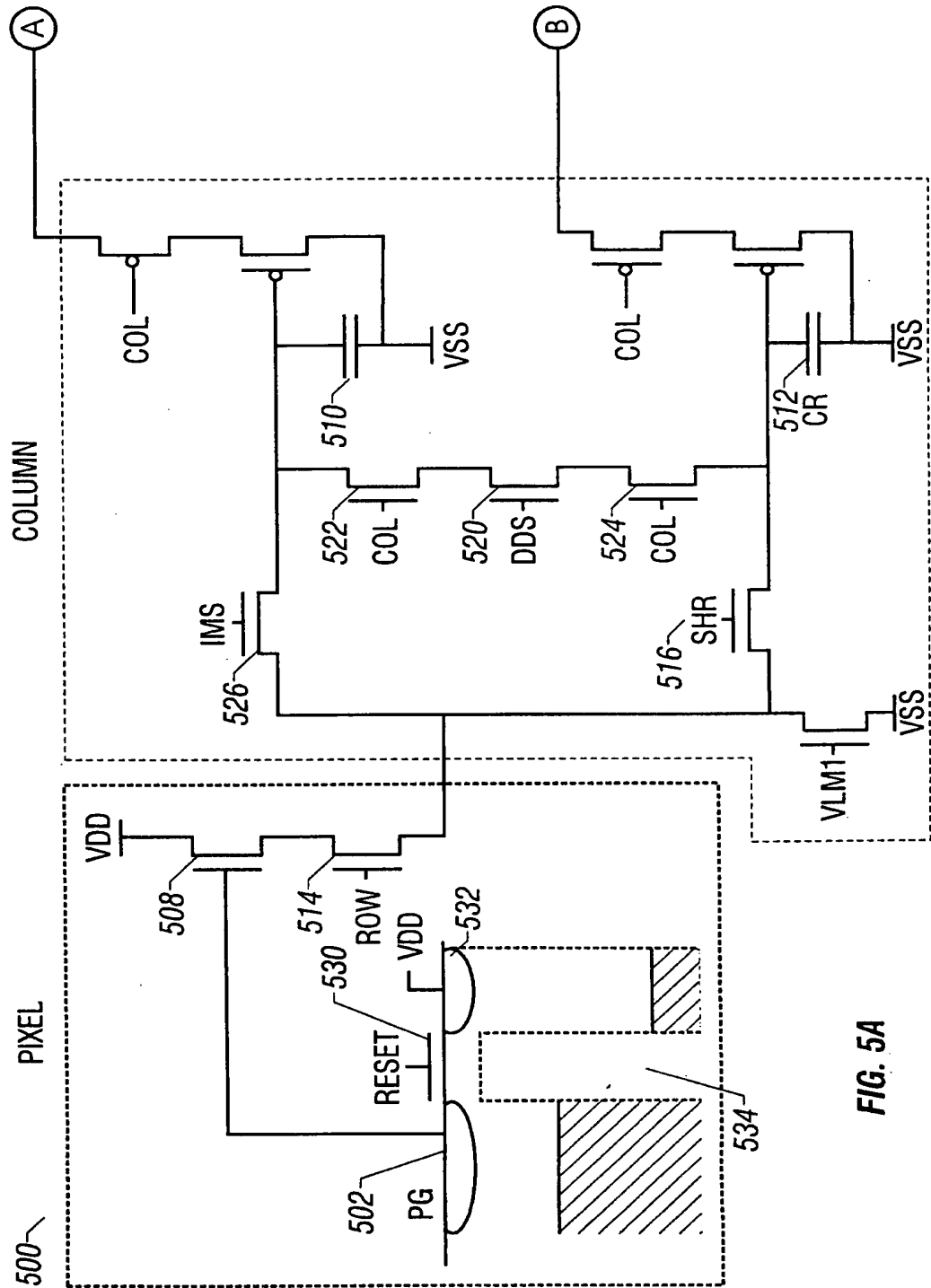


**FIG. 4A**



**FIG. 4B**

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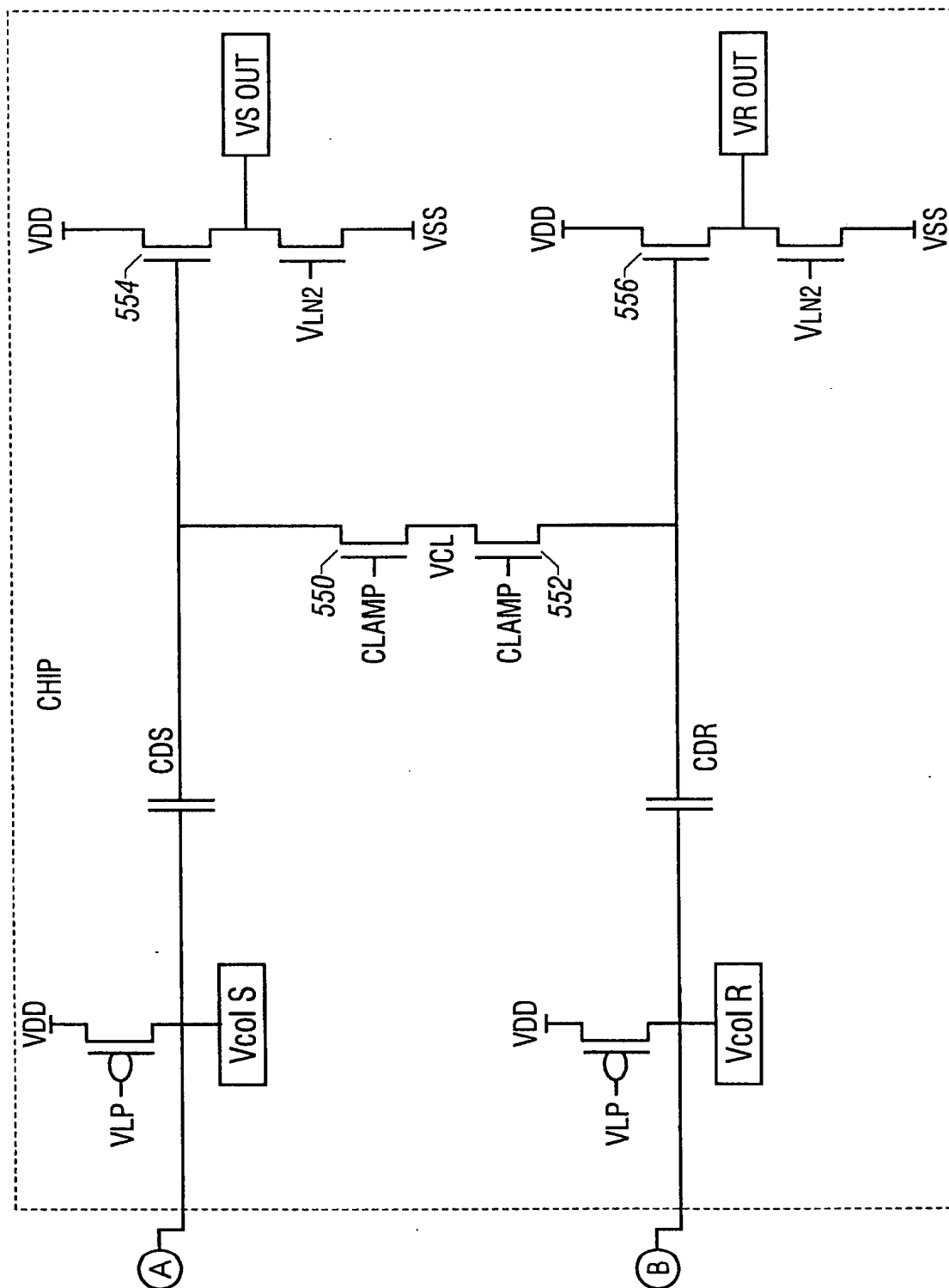


FIG. 5B



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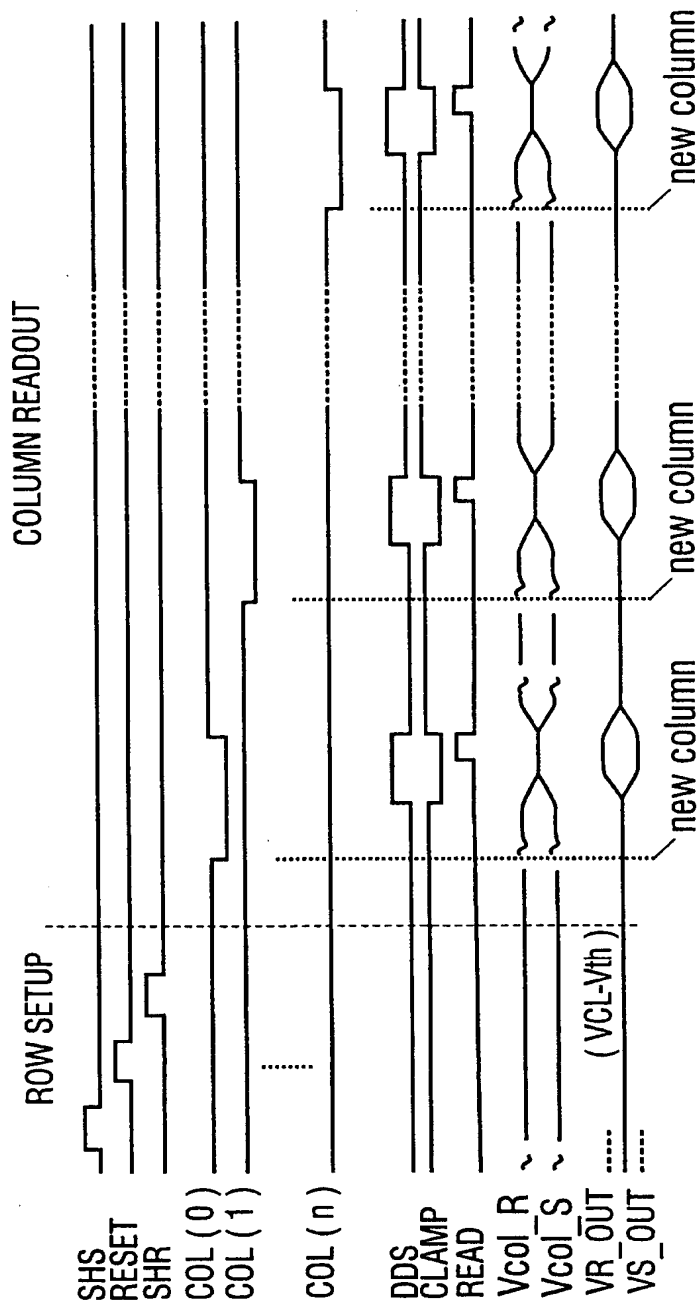


FIG. 6



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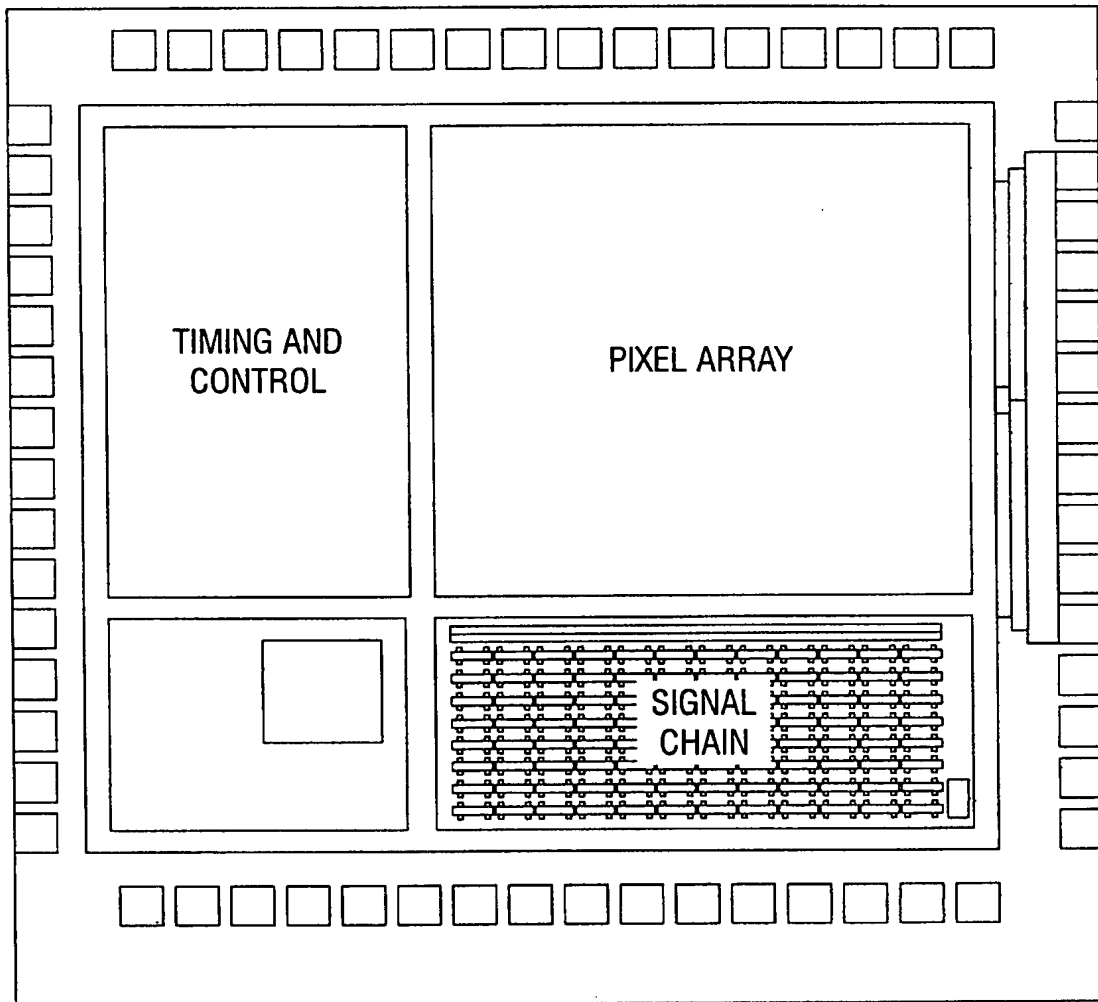


FIG. 7



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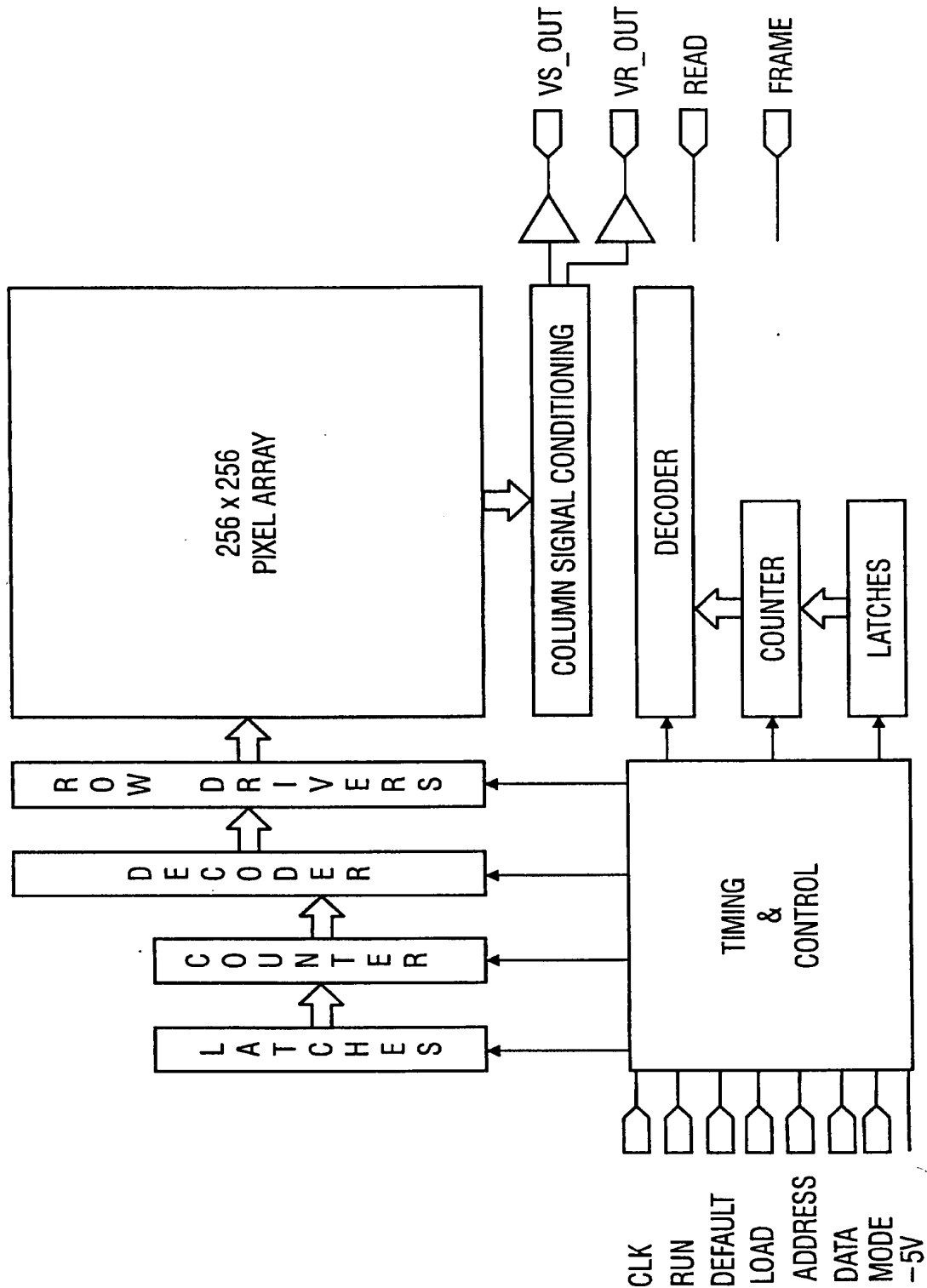
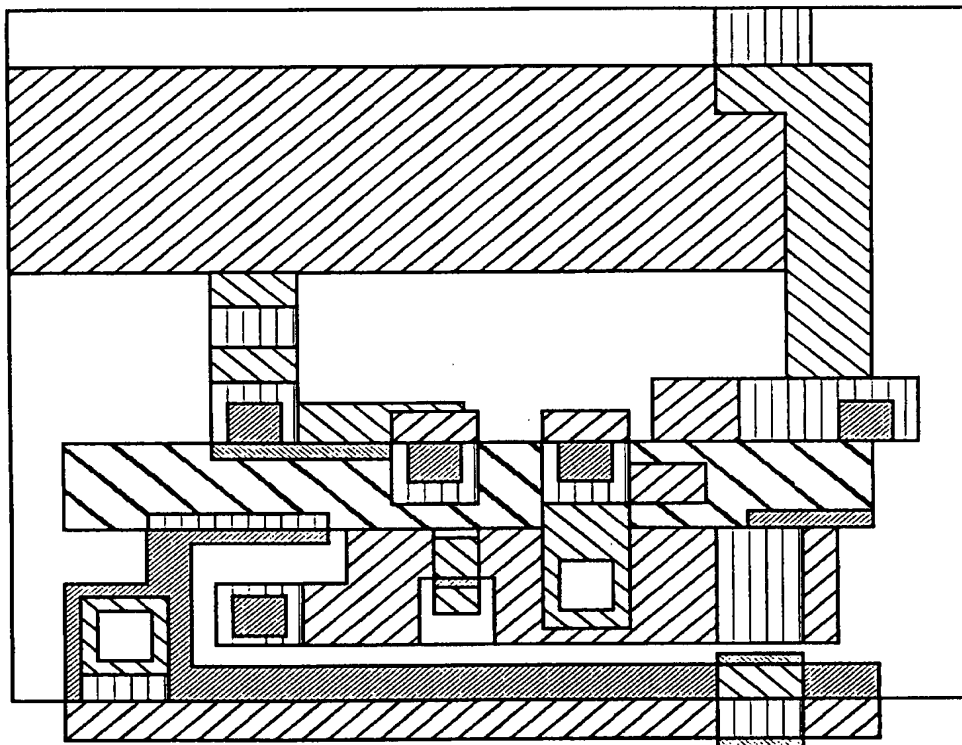


FIG. 8

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|                           |  |
|---------------------------|--|
| Array Size                | 256 x 256  |
| Pixel Size                | 20.4 $\mu\text{m}$   |
| Technology                | 1.2 $\mu\text{m}$ n-well CMOS ( HP )                         |
| Maximum Clock Rate        | 10 MHz   |
| Minimum Clock Rate        | none   |
| Maximum Pixel Rate        | 2.5 MHz  |
| Maximum Integration Delay | 16 x 10 <sup>9</sup> clock periods<br>or 1600 secs at 10 MHz |

FIG. 9